REMARKS

Claims 1-15 and 24-27 were pending in the Application. Claim 1 is an independent claim and claims 2-9 depend therefrom. Claim 10 is an independent claim and claims 11-12 depend therefrom. Claim 13 is an independent claim and claims 14-15 depend therefrom. Claim 24 is an independent claim and claims 25-27 depend therefrom. Claims 16-23 and 28-40 were previously canceled. Applicant respectfully requests reconsideration of the application in light of the above amendments and the following remarks.

Rejections Under 35 U.S.C. §112, First Paragraph

Claims 1-15 and 25-27 were rejected under 35 U.S.C. §112, first paragraph, as allegedly failing to comply with the written description requirement. Specifically, "[t]he examiner has not found to [sic] support in Applicant's Specification for the newly amended limitation of 'a first [logic] circuit associated exclusively with a first memory block' in claims 1, 10, and 13." (Non-Final Office Action, Pages 2-3, Point 4 (emphasis in original)). The Applicant respectfully traverses the above-mentioned rejection for at least the following reasons.

Although the Applicant's Specification does not specifically use the term "exclusively," support for "a first logic circuit associated exclusively with a first memory block" is repeatedly disclosed throughout the Applicant's specification. For example, with regard to Applicant's Figure 1, the Applicant's Specification states at Paragraph [31] that "[t]he second set of flags 150 includes **a first flag 151 that corresponds to the first memory block 120** and **a second flag 152 that corresponds to the second memory block 130**." Additionally, Applicant's Specification states the following at Paragraph [33]:

> **The second set of flags 150 contains a flag 151, 152 corresponding to each memory block 120, 130.** These memory block flags 151, 152 indicate whether **each flag's corresponding memory block** 120, 130 contains a memory segment that is available for data storage. **For example, the first block flag 151**

> **corresponds to the first memory block 120**. The first block flag 151 contains an indication (*e.g.*, "No") to indicate that none of the memory segments 121-124 in the first memory block 120 are available for storage. By comparison, **the second block flag 152, which corresponds to the second memory block 130**, contains an indication (*e.g.*, "Yes") to indicate that at least one of the memory segments 131-134 in the second memory block 130 (namely the second memory segment 132) is available for data storage.

(Applicant's Specification, Paragraph [33] (emphasis added)). The Applicant notes that the Applicant's Specification does not disclose the first block flag 151 corresponding to any other memory block other than the first memory block 120. Because Applicant's Specification clearly shows that a first logic circuit (e.g., first block flag 151) is associated exclusively with a first memory block (e.g., memory block 120), the Applicant's Specification clearly supports the use of the term "exclusively." The Applicant notes that further support can be found in the Applicant's Specification, for example, at Figure 2 (first logic circuit 261 and first memory block 221), Figure 3 (first logic circuit 351 and first memory block 370), Figure 4 (first logic circuit 451 and first memory block 411), Paragraphs [40], [47] and [67], among other places. Thus, because the Applicant's Specification clearly supports "a first logic circuit associated exclusively with a first memory block," as recited in Applicant's independent claims 1, 10, and 13, the rejections of claims 1-15 and 25-27 under 35 U.S.C. §112, first paragraph, cannot be maintained. The Applicant respectfully requests that the rejections of claims 1-15 and 25-27 under 35 U.S.C. §112, first paragraph, be withdrawn.

Rejections Under 35 U.S.C. §103(a) – Goldberg and Lehman (Claims 1-15)

Claims 1-15 were rejected under 35 U.S.C. §103(a) as being unpatentable over Goldberg (U.S. Patent No. 6,874,062) in view of Lehman (U.S. Patent No. 6,658,437). The Applicant respectfully traverses the above-mentioned rejections for at least the following reasons.

In order for a *prima facie* case of obviousness to be established, the Manual of Patent Examining Procedure, Rev. 6, Sep. 2007 ("MPEP") states the following:

> The key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious. The Supreme Court in KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385, 1396 (2007) noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made explicit. The Federal Circuit has stated that "rejections on obviousness cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness."

See the MPEP at § 2142, citing *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006), and *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d at 1396 (quoting Federal Circuit statement with approval). Further, MPEP § 2143.01 states that "the mere fact that references can be combined or modified does not render the resultant combination obvious unless the results would have been predictable to one of ordinary skill in the art" (citing *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d 1385, 1396 (2007)). Additionally, if a *prima facie* case of obviousness is not established, the Applicant is under no obligation to submit evidence of nonobviousness:

> The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness.

See MPEP at § 2142.

Regarding claim 1, Applicant respectfully submits that the proposed combination of references fails to teach, suggest, or disclose at least, for example, "a first logic circuit associated exclusively with a first memory block of the plurality of memory blocks, the first logic circuit having a first state when the first memory block has a memory segment that is available for data storage and a second state when the first memory block does not have a memory segment that is available for data storage, wherein the first state comprises at least a portion of a memory address of the first memory block," as set forth in Applicant's amended, independent claim 1.

Regarding claim 10, Applicant respectfully submits that the proposed combination of references fails to teach, suggest, or disclose at least, for example, "a first logic circuit associated exclusively with a first memory block of the plurality of memory blocks, the first logic circuit

having a first state when the first memory block has a memory segment that is available for data storage and a second state when the first memory block does not have a memory segment that is available for data storage; wherein the first state of the first logic circuit comprises a number of available memory segments in the first memory block," as set forth in Applicant's amended, independent claim 10.

Regarding claim 13, Applicant respectfully submits that the proposed combination of references fails to teach, suggest, or disclose at least, for example, "a first logic circuit associated exclusively with a first memory block of the plurality of memory blocks, the first logic circuit having a first state when the first memory block has a memory segment that is available for data storage and a second state when the first memory block does not have a memory segment that is available for data storage; wherein the second state of the first logic circuit comprises information indicating an offset to available memory," as set forth in Applicant's amended, independent claim 13.

A. Response to First Point of Argument in the Non-Final Office Action

Points 26-29 of the non-final Office Action address the Applicant's argument that the combination of Goldberg in view of Lehman fail to disclose "the first state comprises at least a portion of a memory address of the first memory block," as set forth in Applicant's independent claim 1. It appears from the arguments presented in Points 26-29 of the non-final Office Action that the Examiner agrees that Goldberg fails to "explicitly disclose the details of having the first state include at least a portion of a memory address of the first memory block" (Non-Final Office Action, Page 6, Lines 12-13) and Lehman merely discloses determining the address of a block based on bit position in the base group. (*See* Non-Final Office Action, Page 20, Lines 22-23; Page 21, Lines 5-6 and 12-16). Instead, it appears from the arguments presented in Points 26-29 of the non-final Office Action that the Examiner is arguing that the Examiner is broadly interpreting "the first state comprises" to mean "the bit position of the first state." (*See* Non-Final Office Action, Page 20, Lines 1-5 and 22-23; Page 21, Lines 5-6 and 12-16). As discussed in

more detail below, such an interpretation is clearly contrary to the claim language used and is further distinguished in the Applicant's Specification.

The Applicant appreciates the Examiner's recognition that Lehman discloses "the address position 8 has a state of 0...." (Non-Final Office Action, Page 20, Lines 22-23). In other words, Lehman's first state comprises "0." The Applicant notes that "0" is not "at least a portion of a memory address of the first memory block." Rather, "0" merely indicates that a memory unit is available. In order for Lehman to determine the address of the state "0," Lehman needs to look to the bit position of the state "0". Thus, the state "0" itself, does not comprise "at least a portion of a memory address of the first memory block." Instead, the bit position of the state "0" provides the address of the state "0." The Applicant notes that Applicant's independent claim 1 does **not** recite "wherein **a bit position of the first state is used to determine** at least a portion of a memory address of the first memory block." Rather, Applicant's independent claim 1 recites "wherein **the first state comprises** at least a portion of a memory address of the first memory block." Lehman clearly fails to disclose "wherein **the first state comprises** at least a portion of a memory address of the first memory block," as set forth in Applicant's independent claim 1.

The Applicant further notes that Lehman's "bit position" is not "at least a portion of a memory address." Lehman teaches "[t]he address of a block **is determined by** the bit position in the base group and by the position of the base group in the larger allocation array." (Lehman, Column 10, Lines 56-58 (emphasis added)). Thus, although Lehman teaches that "[t]he address of a block **is determined by** the bit position," **the bit position itself is not** "at least a portion of a memory address." Therefore, Lehman's teaching of "[t]he address of a block **is determined by** the bit position," cannot disclose "the first state **comprises at least a portion of a memory address** of the first memory block," as set forth in Applicant's independent claim 1.

The Applicant also notes that the term "comprises" is synonymous with "contains." (*See* MPEP 2111.03). Thus, by reciting "the first state **comprises at least a portion of a memory address** of the first memory block," the Applicant notes that in order to teach the claim limitation, Lehman would have to disclose its state "0" actually containing at least a portion of a memory

address. Clearly, "0" does not contain at least a portion of a memory address. Further, even if "0" could be interpreted as "containing" a bit position (which it cannot), as shown above, Lehman's **bit position itself** is not a memory address. Rather, as discussed above, Lehman's bit position is **used to determine** the address of a block. Thus, giving Applicant's independent claim 1 it broadest reasonable interpretation, one of ordinary skill in the art would not confuse Lehman's disclosure of determining the block address using the bit position with "the first state comprises at least a portion of a memory address of the first memory block," as set forth in Applicant's independent claim 1.

Further, Point 29 of the non-final Office Action states the following:

> Furthermore, Applicant's specification recites ["the address-determining step 1040 may be accomplished in a variety of ways. For example, various information may be **contained in the segment or block flags** that the step 1040 may utilize to calculate [the] segment address" (Specification, par. 96)] wherein Applicant should note that **this recitation does not distinguish Applicant's invention** from the combination of Goldberg and Lehman since **Lehman describes determining address portions of memory segments based on the position of the identified available bits**....

(Non-Final Office Action, Page 21, Lines 7-13). The Applicant respectfully disagrees. Paragraph [96] of Applicant's Specification states the following:

> The address-determining step 1040 determines an address of the available memory segment corresponding to the previously-identified segment flag and optionally, the previously-identified block flag. **The address-determining step 1040 may be accomplished in a variety of ways. For example, various information may be contained in the segment or block flags that the step 1040 may utilize to calculate the segment address.** *Alternatively, for example, the step 1040 may convert the position of the identified segment flag in the set of segment flags to the address of the memory segment. **Alternatively**, for example, **the step 1040 may also utilize the position of the identified block flag in the set of block flags to determine a portion of the available memory segment's address**.*

(Applicant's Specification, Page 29, Paragraph [96], Lines 3-11 (emphasis added)). Clearly, the Applicant's Specification discloses "a variety of ways" for determining the address. One such way is where information is actually contained in the segment or block flag (i.e., "**the first state**

comprises at least a portion of a memory address of the first memory block"). Another completely different way to determine the address is to **utilize the position of the identified block flag**. Clearly, a portion of the memory address being contained in the state is distinguishable from using the position of the state to determine a portion of the available memory segment's address. Thus, Lehman's teaching of "[t]he address block is determined by the bit position in the base group and by the position of the base group in the larger allocation array" fails to disclose "**the first state comprises at least a portion of a memory address** of the first memory block," as recited in Applicant's independent claim 1.

Nowhere in the combination of Goldberg and Lehman is there any disclosure of "the first state comprises at least a portion of a memory address of the first memory block," as set forth in Applicant's independent claim 1. The cited sections of Lehman in the non-final Office Action (e.g., Col. 10, line 50-Col. 11, line 15; Col. 11, lines 38-46; Figure 7 and related text; Figure 9 and related text), all discuss assigning an address to a bit based on the position of the bit. A bit position being associated with an address is different than "**the first state comprises** at least a portion of a memory address." Because the combination of Goldberg in view of Lehman fails to teach or suggest all the claim limitations, a rejection under 35 U.S.C. §103(a) cannot be maintained.

B. Response to Second and Third Points of Argument in the Non-Final Office Action

Points 30-33 of the non-final Office Action address the Applicant's argument that there is no motivation to combine Goldberg and Lehman because Goldberg clearly teaches away from using multiple buffer pools as taught by Lehman. The Applicant notes that a disclosure that criticizes, discredits, or otherwise discourages the solution claimed of a second disclosure, teaches away from the combination of disclosures. *In re Fulton*, 391, F.3d 1195, 1201 (Fed. Cir. 2004). Contrary to the non-final Office Action's assertion otherwise (*See* Non-Final Office Action, Page 22, Lines 6-10), Goldberg clearly criticizes, discredits and otherwise discourages optimizing memory allocation using multiple buffer pools as taught by Lehman. For example,

Goldberg explicitly states that the use of multiple buffer pools as taught by Lehman "results in a considerable waste of storage space." (Goldberg, Column 2, Lines 34-35). One skilled in the art, upon reading Goldberg, would clearly be discouraged from using multiple buffer pools to optimize memory allocation as taught by Lehman. Thus, despite Lehman's efforts to make multiple buffer pool implementations require less space to store allocation information, one skilled in the art would not have found that the combined teachings of Goldberg and Lehman suggest Applicant's claim limitations because Goldberg teaches staying away from multiple buffer pool implementations altogether. Additionally, as mentioned above in Point A, even if Goldberg and Lehman were combinable, the combination of reference still fails to teach or suggest all the claim limitations.

The Applicant also notes that with regard to the non-final Office Action's citation to MPEP 2123, that Goldberg does not disclose multiple buffer pools as a non-preferred (or preferred) embodiment. Rather, as discussed above, Goldberg teaches staying away from multiple buffer pool implementations altogether. Thus, MPEP 2123 is inapplicable to the present situation.

Because the combined teaching of Goldberg and Lehman would not have been construed by one skilled in the art as suggesting the limitations of Applicant's claims, the rejection under 35 U.S.C. §103(a) cannot be maintained.

C. Response to Fourth Point of Argument in the Non-Final Office Action

Points 34-36 of the non-final Office Action address the Applicant's argument that the combination of Goldberg in view of Lehman fail to disclose "wherein the first state of the first logic circuit comprises a number of available memory segments in the first memory block," as set forth in Applicant's independent claim 10. It appears from the arguments presented in Points 34-36 of the non-final Office Action that the Examiner is interpreting Lehman's "bit string 1111 1100 0000 0011" to be Applicant's "wherein the first state of the first logic circuit comprises a

number of available memory segments in the first memory block." (*See* Non-Final Office Action, Page 20, Lines 1-5 and 22-23; Page 21, Lines 5-6 and 12-16). However, such an interpretation is clearly contrary to Applicant's claim language. For example, Applicant's independent claim 10 states that "the first logic circuit having a first state when any of the memory segments of the first memory block are available for data storage and a second state when none of the memory segments of the first memory block are available for storage." Lehman discloses that each bit signifies a state (i.e., available or unavailable) of a memory block. In other words, Lehman discloses that each bit is a separate logic circuit having a state of "0" or "1" depending on whether the logic circuit detected an available segment to which it corresponds.

Nowhere in Lehman is there any disclosure of an additional logic circuit that represents a first state corresponding to all of the states of the plurality of logic circuits that correspond to each of the memory blocks in Lehman. Thus, Lehman merely discloses a plurality of logic circuits, each of the logic circuits having a state corresponding to the availability of a memory block. Therefore, Lehman cannot disclose "wherein the first state of the first logic circuit comprises a number of available memory segments in the first memory block," because Lehman does not disclose, for example, wherein the first state (e.g., state "0") of the first logic circuit (e.g., the logic circuit corresponding to the bit position 8) comprises a number of available memory segments in the first memory block.

Also, even if Lehman's disclosure of a bit string 1111 1100 0000 0011 could be a state of a first logic circuit (which it cannot), the above-mentioned bit stream would have a different state then, for example, bit string 0011 0011 0011 0011, yet both bit strings show available segments. In other words, even if Lehman's entire bit string was a state, Lehman still fails to disclose "the first logic circuit **having a first state when any of the memory segments of the first memory block are available for data storage**." Instead, Lehman would disclose a first logic circuit having a plurality of states when any of the memory segments of the first memory block are available for data storage.

Clearly, the combination of Goldberg and Lehman fails to disclose "wherein **the first state of the first logic circuit comprises a number of available memory segments** in the first memory block," as set forth in Applicant's amended, independent claim 10. Rather, Lehman teaches looking at an entire bit map to count up the number "0" bits in the bit map. As stated in Lehman, "logical groups inside the 16 bits must be determined **by examining adjacent bits**." (Lehman, Column 11, Lines 8-9). Thus, Lehman does not teach "**the first state of the first logic circuit comprises a number of available memory segments in the first memory block**" wherein the "first logic circuit [is] associated **exclusively** with [the] first memory block." Further, the Applicant appreciates the Examiner's recognition that "Goldberd [sic] does not expressly disclose the details of wherein the first state of the first logic circuit comprises information indicating a number of available memory segments in the first memory block." (Non-Final Office Action, Page 14, Line 22 through Page 15, Line 2). Because the combination of Goldberg in view of Lehman fails to teach or suggest all the claim limitations, a rejection under 35 U.S.C. §103(a) cannot be maintained.

D. Response to Fifth Point of Argument in the Non-Final Office Action

Points 37-38 of the non-final Office Action address the Applicant's argument that the combination of Goldberg in view of Lehman fail to disclose "a first logic circuit associated **exclusively** with a first memory block...wherein the second state of the first logic circuit comprises information indicating an offset to available memory," as set forth in Applicant's independent claim 13. It appears from the arguments presented in Points 37-38 of the non-final Office Action that the Examiner is interpreting Lehman's "pointer array 124" to be Applicant's "a first logic circuit associated **exclusively** with a first memory block...wherein the second state of the first logic circuit comprises information indicating an offset to available memory." However, Lehman's "pointer array 124" is not a "first logic circuit," let alone "associated exclusively with a first memory block," let alone "having a first state when any of the memory segments of the first memory block are available for data storage and a second state when none of the memory segments of the first memory block are available for storage."

Further, the Examiner's interpretation of "first logic circuit" with regard to Applicant's independent claim 13 is inconsistent. First, the Examiner interprets "first logic circuit" of Applicant's independent claim 13 to be a bit in a LLB as disclosed in Goldberg. (*See* Non-Final Office Action, Page 17, Lines 1-18). Then, the Examiner interprets the "first logic circuit" of Applicant's independent claim 13 to be a pointer array in Lehman. (*See* Non-Final Office Action, page 18, Lines 1-12). Clearly, a bit in a LLB as disclosed in Goldberg is different than a pointer array as disclosed in Lehman. Thus, there is no motivation to combine features of a bit in a LLB with features of a pointer array. Therefore, the combination of Goldberg and Lehman cannot disclose "wherein the second state of the first logic circuit comprises information indicating an offset to available memory." Because the combination of Goldberg in view of Lehman fails to teach or suggest all the claim limitations, a rejection under 35 U.S.C. §103(a) cannot be maintained.

E. Claims 1-15 are Allowable

The Applicant respectfully submits that, based upon the above, the proposed combination of Goldberg in view of Lehman fails to teach or suggest by themselves or in combination all of the limitations of Applicant's independent claims 1, 10 and 13, and that the rejections of claims 1, 10 and 13 under 35 U.S.C. §103(a) cannot be maintained. Therefore, Applicant respectfully requests that the rejections of claims 1, 10 and 13 under 35 U.S.C. §103(a), be withdrawn.

Because dependent claims 2-9, 11-12 and 14-15 depend, directly or indirectly, from independent claim 1, 10 or 13, and because claims 1, 10 and 13 are allowable over the proposed combination of references, the Applicant asserts that claims 2-9, 11-12 and 14-15 are also allowable over the proposed combination of references and that the rejections of dependent claims 2-9, 11-12 and 14-15 are now moot. The Applicant further submits that each of claims 2-9, 11-12 and 14-15 is independently allowable. Thus, the Applicant respectfully requests that the rejections of claims 1-15 under 35 U.S.C. §103(a), be withdrawn.

Rejections Under 35 U.S.C. §102(b) and 103(a) – Goldberg and Lehman (Claims 24-27)

Claim 24 was rejected under 35 U.S.C. §102(b) as being anticipated by Goldberg. Claims 25-27 were rejected under 35 U.S.C. §103(a) as being unpatentable over Goldberg in view of Lehman. The Applicant respectfully traverses the above-mentioned rejections for at least the following reasons.

Regarding claims 24-27, for reasons similar to those stated previously, the Applicant submits that such claims are allowable.

For example and without limitation, for reasons generally analogous to those stated previously with regard to claim 1, the Applicant submits that claim 25 is allowable over Goldberg, and over Goldberg in view of Lehman.

Also for example, for reasons generally analogous to those stated previously with regard to claim 10, the Applicant submits that claim 26 is allowable over Goldberg, and over Goldberg in view of Lehman.

Further for example, for reasons generally analogous to those stated previously with regard to claim 13, the Applicant submits that claim 27 is allowable over Goldberg, and over Goldberg in view of Lehman.

Final Matters

The Office Action makes various statements regarding former claims 1-15 and 24-27, 35 U.S.C. § 102(b), 35 U.S.C. § 103(a), the Goldberg reference, the Lehman reference, one of skill in the art, etc. that are now moot in view of the above-mentioned amendments and/or arguments. Thus, the Applicants will not address all of such statements at the present time. However, the Applicants expressly reserve the right to challenge such statements in the future should the need

arise (e.g., if such statements should become relevant by appearing in a rejection of any current or future claim).

Applicant reserves the right to argue additional reasons supporting the allowability of claims 1-15 and 24-27 should the need arise in the future.

CONCLUSION

Applicant respectfully submits that claims 1-15 and 24-27 are in condition for allowance, and requests that the application be passed to issue.

Should anything remain in order to place the present application in condition for allowance, the Examiner is kindly invited to contact the undersigned at the telephone number listed below.

Please charge any required fees not paid herewith or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Date: December 8, 2008

Respectfully submitted,

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